REMARKS

Claims 18-27 are pending in the present application. Claims 18, 22 and 25-27 have been amended. Claims 1-17 and 28-32 have been canceled. Applicant respectfully reserves the right to file a divisional application for non-elected claims 1-17, 31 and 32.

Drawings

Applicant notes the Examiner's acceptance of the drawings as filed along with the present application on January 5, 2004.

Substitute Specification

A Substitute Specification including an abstract has been submitted herewith. Also enclosed is a marked-up version of the Substitute Specification. Applicant respectfully submits that no new matter has been entered via the Substitute Specification. **The Examiner is respectfully requested to enter the Substitute Specification as of record.**

Claim Rejections-35 U.S.C. 102

Claims 18-30 have been rejected under 35 U.S.C. 102(b) as being anticipated by the Chang et al. reference (U.S. Patent No. 6,486,028). This rejection is respectfully

traversed for the following reasons.

The non-volatile memory array having vertical transistors of claim 18 features that each of the vertical transistors include in combination a first doping region "of a first conductive type being underneath a bottom of the trench"; a second doping region "of the first conductive type being beside a top of the trench"; a third doping region "of a second conductive type beside the trench"; a fourth doping region "of the first conductive type beside the trench, and being located lower than the third doping region"; a gate dielectric layer; and a conductive plug, "wherein the first doping regions of the vertical transistors are connected as a common plate serving as one of a common source and a common drain". Applicant respectfully submits that the Chang et al. reference as relied upon by the Examiner does not disclose these features.

Claim 18 has been amended to include features somewhat similar to that as in original dependent claims 28-30. With respect to claim 29, the Examiner has very generally asserted on page 4 of the current Office Action dated July 7, 2005, that column 3, lines 31-37 and column 4, lines 43-47 of the Chang et al. reference discloses vertical transistors including "a fourth doping region (channel regions) of the first conductive type beside the trench, and the third doping region (channel regions) is located higher than the fourth doping region (channel regions)".

However, column 3, lines 31-34 of the Chang et al. reference as specifically relied upon by the Examiner describes with respect to Fig. 1: "A channel threshold adjust implantation (not shown) is then performed using a typical tilt angle implantation

technique using, for example, boron or boron fluoride ions for NMOS devices or, for example, arsenic or phosphorus ions for PMOS devices...". Applicant emphasizes that boron or boron fluoride ions as implanted have p-type conductivity, and arsenic or phosphorus ions as implanted have n-type conductivity.

Applicant thus emphasizes that the channel threshold adjust implantation described in the above noted portion of the Chang et al. reference dopes the channel with ions having a conductivity type opposite that of the corresponding source/drain regions. For example, p-type boron or boron fluoride ions are implanted into the channel region of an NMOS device having n-type source/drain regions. Accordingly, it is not understood how column 3, lines 31-37 of the Chang et al. reference as particularly relied upon by the Examiner can be interpreted to disclose or suggest a fourth doping region having first conductivity type that is the same as source/drain regions of the device, as would be necessary to meet the features of claim 18.

Moreover, column 4, lines 43-47 of the Chang et al. reference as further specifically relied upon by the Examiner as noted above, describes that the NROM is a vertical structure, the channels are also in a vertical direction, and that the bit lines are consequently formed to allow further size reduction of the NROM cell. However, this particular portion of the Chang et al. reference as specifically relied upon by the Examiner does not disclose or even remotely suggest a fourth doping region having a first conductivity type that is the same as source/drain regions of the device, as would be necessary to meet the features of claim 18. Accordingly, Applicant respectfully

submits that the non-volatile memory array having vertical transistors of claim 18 distinguishes over the Chang et al. reference as relied upon by the Examiner, and that this rejection of claims 18-27 is improper for at least these reasons.

With further regard to this rejection, claim 18 as noted above features in combination first, second, third and fourth doping regions. However, Figs. 3-6 of the Chang et al. reference merely illustrate at most three doping regions, whereby "doping region" 100 serves as a channel for two other "doping regions" 106 and 108. Clearly, Figs. 3-6 of the Chang et al. reference do not include or illustrate a fourth doping region, in addition to first through third doping regions, as would be necessary to meet the features of claim 18. Applicant therefore respectfully submits that the non-volatile memory array having vertical transistors of claim 18 distinguishes over the Chang et al. reference as relied upon by the Examiner, and that this rejection of claims 18-27 is improper for at least these additional reasons.

With still further regard to this rejection, the Examiner has very generally asserted on page 4 of the current Office Action with respect to claim 30, that the Chang et al. reference discloses in column 3, lines 38-52 first doping regions of vertical transistors connected as one of a common source and a common drain. However, as described in column 3, lines 37-42 of the Chang et al. reference as specifically relied upon by the Examiner: "Referring to FIG. 2, an ion implantation 103 is performed to form a first source/drain region 104, and a second source/drain region 106 within the substrate 100 in the upper corners of the trench 102, and to form a ***common***

source/drain region 108 within the substrate 100 at a bottom of the trench 102" (our emphasis added).

Applicant respectfully submits that the word "***common***" in the above noted portion of the Chang et al. reference as specifically relied upon by the Examiner should be understood to mean that region 108 functions at the same time as both a source and a drain for neighboring transistors. This should be readily understood in view of Figs. 2-6 of the Chang et al. reference, because N+ region 108 does not extend to be connected to any adjacent N+ regions 108. In contrast, and as noted merely as an example so as not to be construed as limiting, Fig. 12 of the present application shows doping regions below the trenches as connected together as a plate. The Chang et al. reference as relied upon by the Examiner does not disclose first doping regions of vertical transistors that are connected together as a common plate so as to serve as one of a common source and a common drain, as would be necessary to meet the features of claim 18. Applicant therefore respectfully submits that the non-volatile memory array having vertical transistors of claim 18 distinguishes over the Chang et al. reference as relied upon by the Examiner, and that this rejection of claims 18-27 is improper for at least these additional reasons.

Conclusion

The Examiner is respectfully requested to reconsider and withdraw the corresponding rejection, and to pass the claims of the present application to issue, for

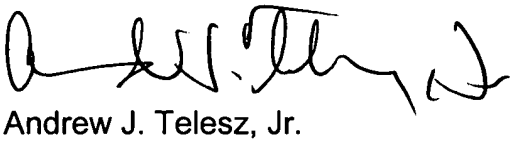
at least the above reasons.

In the event that there are any outstanding matters remaining in the present application, please contact Andrew J. Telesz, Jr. (Reg. No. 33,581) at (571) 283-0720 in the Washington, D.C. area, to discuss these matters.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment for any additional fees that may be required, or credit any overpayment, to Deposit Account No. 50-0238.

Respectfully submitted,

VOLENTINE FRANCOS & WHITT, P.L.L.C.



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Enclosures: Substitute Specification
Marked-Up Version of Substitute Specification